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Design of D-Latch Using Three Transistor NAND Gates in Mentor Graphics 130nm

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ABSTRACT: Flip-flops and latches are used as a memory factor for information storing. In case of latches the output modifications when the allow sign is asserted (when the enable signal is active the output modifications when the input changes) whereas in case of Flip-flops the output modifications as the rising or the falling off the clock pulse. The output doesn't trade before or after the rising area or the falling edge. So, the latches are called stage triggering circuit. And the flip-flops are known as edge triggering circuit. A Flip-flop can save a single bit of data: "0" and "1" in its two states. This state can be used in describing in a sequential common sense in which the output and the next stage depend on the existing enter and the cutting-edge state. Thus, Flip-flops can be used for counting the number of clock pulses. Current lookup focuses to implement the D latch with three transistor NAND gate in 130nm science the usage of mentor graphics. And compares the existed d latch and proposed D latch on the groundwork of electricity dissipation and area reduction. This is due to the fact power dissipation is low there will be low warmth dissipation. Increase battery existence and make the circuit extra dependable and breakdown of the circuit will be low.

KEYWORDS: D Latch, FlipFlops,Low Power.

I. INTRODUCTION

Flip-flops and latches are basic fundamental circuit of digital electronics system which is used in communication computer and many other systems. A Flip-flops and latches have a two state so it is called bi-stable multi-vibrator.

A. D Latch

This is the most basic circuit of D latches in S-R latch we have two input, whereas in D latches only one input is used. At the input of S-R a not gate is connected between S and R. In D-latch Two and gates are required. The NAND gate which has step input of the not gate corresponded to the output Q. And other to the Q'. The fig 1 shows the circuit diagram.

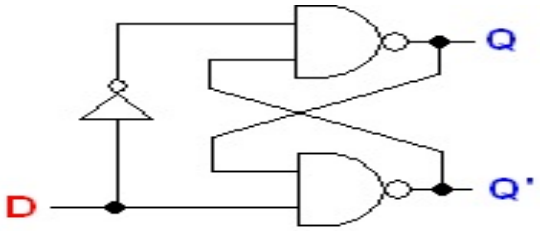

Fig 1.1: D latch

In modern electronic systems, CMOS latches and Flip-Flops (FFs) are responsible for the data flow and data storage. Since the beginning of research on emerging devices, a wide range of latches and FFs have been developed and presented in literature using a variety of non-CMOS devices to complement conventional silicon designs [6]. However, the quest for sequential circuits, designed using non-CMOS devices and operating at high frequencies, still continues.

Ballistic Deflection Transistors (BDTs) are intentionally developed as a high-speed supplement to conventional Si MOSFET systems [7]. They are recent entrant into the emerging nanoscale devices that were experimentally proven to operate at THz frequencies [8]. Significant research in these nanoscale devices has been done during last few years. Current transport modeling, geometry effects on the performance and leakage current mechanisms of BDTs at room

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temperature have been studied [9]. It has been observed that with proper bias conditions, even a single BDT can act as a logic gate. A two input NAND gate of this nanodevice structure indicates the possibility of creation of any logicfunction. A simple, compact fit based analytical model of BDT has been developed to aid the circuit design. The effect of dielectric materials when integrated with BDTs has been studied and is presented.

A.1. Mentor graphics

The Mentor Graphics software package consists of a large number of executable files, documents, libraries, and other components. The locations of these files vary from system to system, so it is necessary to incorporate some mechanism for handling the differences that naturally occur between the installations at different sites. Many of these details are handled using start-up scripts and environment variables. Although these startup scripts simplify the use of the software for the end user, it may be necessary for the user to do some minor editing of start-up files before the software can be used.

The principle of switching a current flow between terminals has been around since at least 1992, when Palm and Thylén proposed a Y-branch junction (YBJ) fabricated in a 2DEG and controlled by an applied electric field. Palm and Thylén later expanded on this work to develop a number of logic functions using these devices, which included an inverter, NAND and NOR gate [10]. Since the publication of that expansion, YBJs have been thoroughly examined and used in a number of novel ways, including the generation of complementary outputs [9], rectification. and even the design of a half-adder [8]. Indeed, the BDT may also be seen as an extension of the YBJ concept, with an additional pull-up potential through the upper center drain, although the primary motivation for the BDT was Song's ballistic rectifier [3]. Tbranch junctions (TBJs) have also been used to create logic functionality, for example using the center branch of the TBJ to pinch off a conductive channel, creating a NAND gate. NAND functionality has also been created using a quantum wire with two co-planar gates, a method with excellent integration density.

II. EXISTING SYSTEM

A NAND gate is a device that performs the negation (NOT) of an AND logic operation — thus the NAND designation. It is one of the fundamental logic gates in digital circuits. In fact it can be proved that ANY logic operation can be done solely with NAND gates. That is, the NAND gate is a "sufficient" gate or an "universal" gate. In modern computers and processors, the NAND gate, as well as other logic gates, are implemented with CMOS circuits. Below is a 4-input NAND gate in CMOS technology. Its advantage, in CMOS version, is a very low energy consumption per operation (it almost doesn't spend energy when the logic values are static) and is implemented with a very small area in silicon chips.

Here below shows the generation of fourtransistor NAND gate in mentor graphics 130nm in step by step processes is shown below.

A. Four transistor NAND gate schematic level

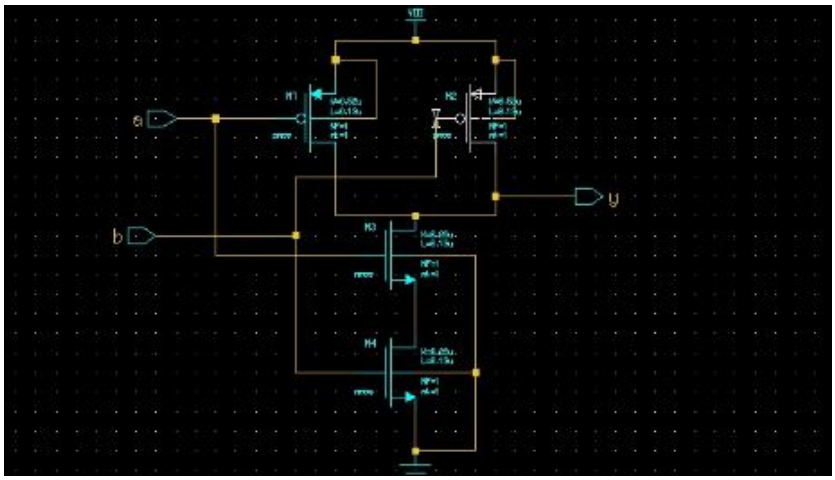

Fig 2.1 Four transistor NAND gate schematic

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NAND gate symbol

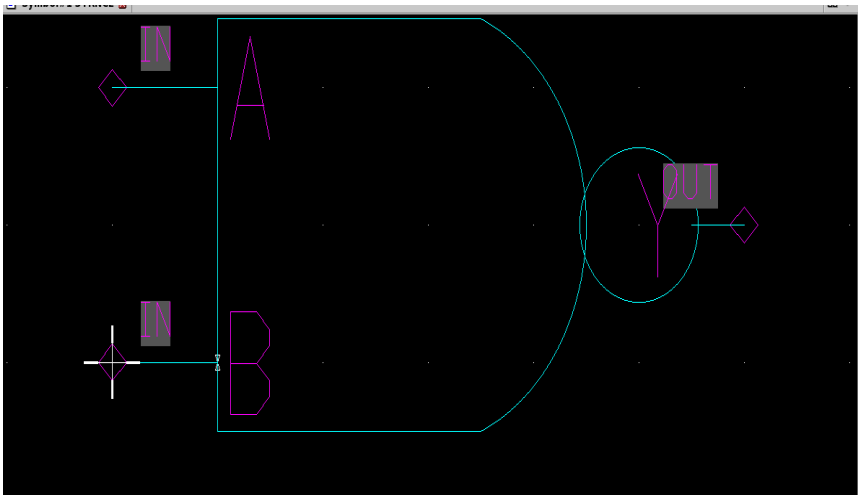

Fig 2.2 NAND Gate symbol

Here below shows the generation of D latch using NAND gate in mentor graphics 130nm in step by step processes and also implemented buffer and it is connected to latch to form D latch

B. D Latch schematic

Here the below shown schematic of D Latch in Mentor 130nm.

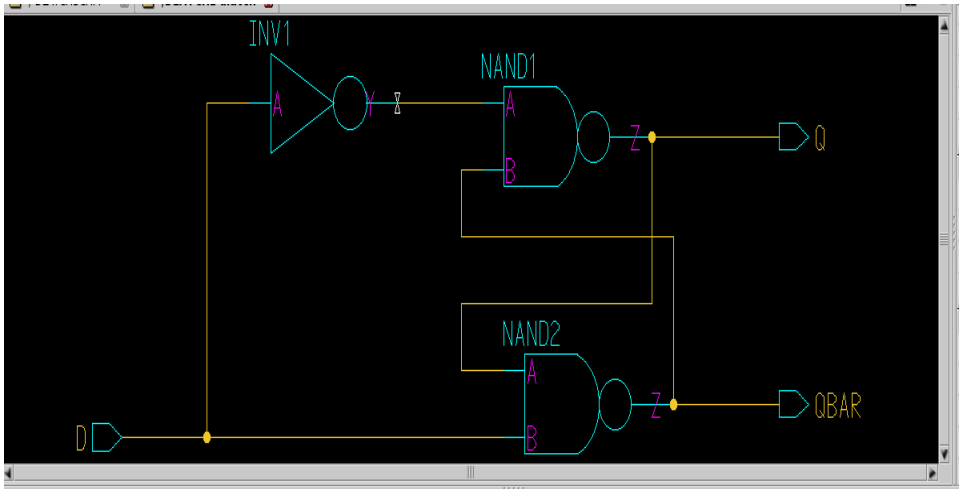

Fig 2.3.D Latch schematic

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B.1 D Latch symbol

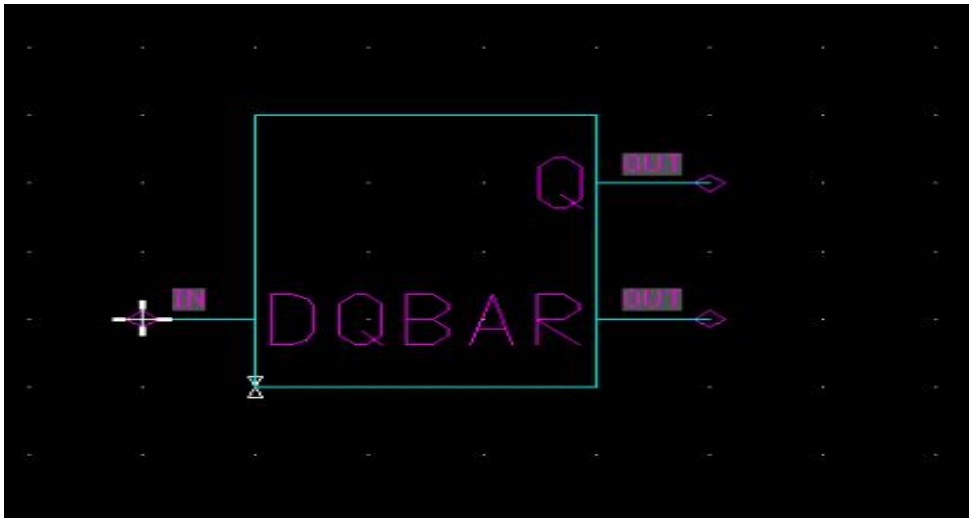

Fig 2.4.D Latch symbol

B.2 D Latch simulation

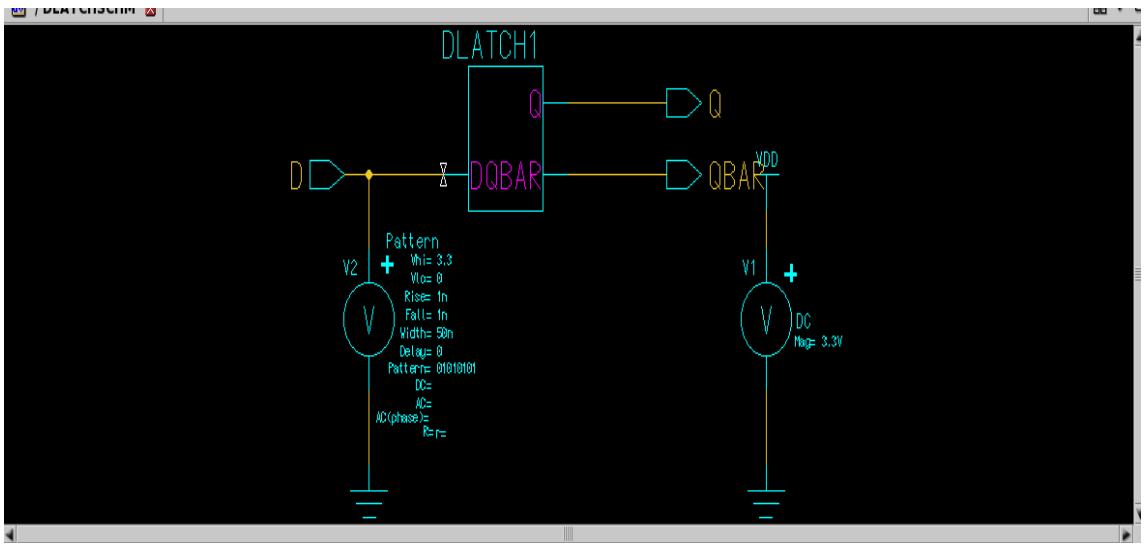

Fig 2.5. D Latch simulation

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B.3 D Latch output waveforms

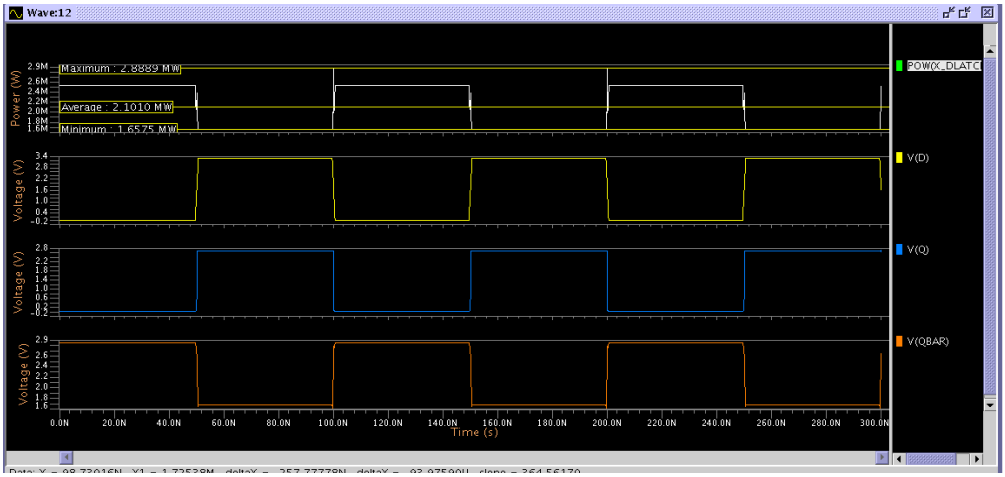

Fig .2.6.D Latch output waveforms

III. PROPOSED SYSTEM

The new design of 3T NAND gate is shown in Figure 3.1. The high-density layout, speed and compact design advantages of PTL and CMOS inverter design style can be utilized efficiently to design 3T NAND circuit. The 3T NAND functionality can be explained as follows.

Here below shows the generation of three transistor NAND gate in mentor graphics 130nm in step by step process in shown below

A. Sschematic level of three transistor NAND gate

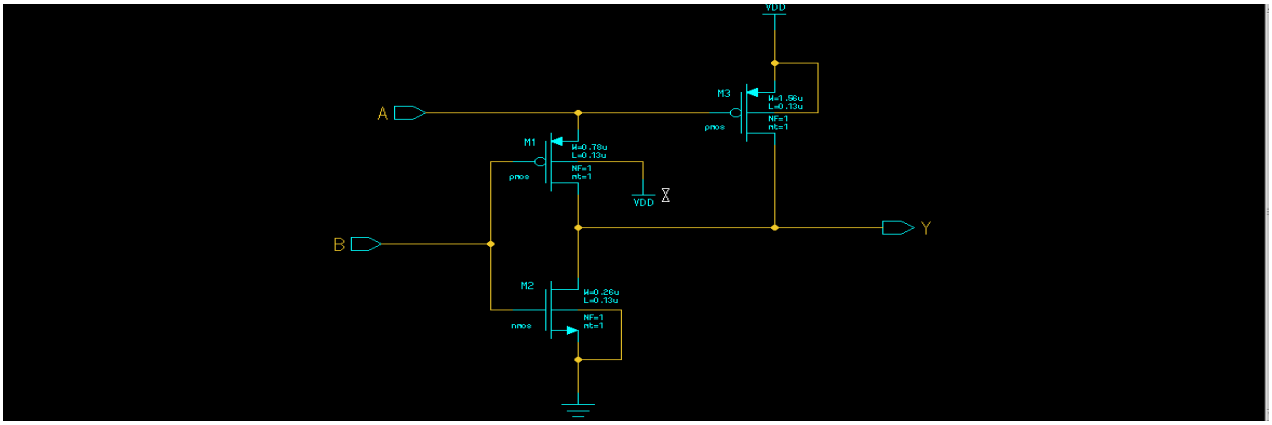

Fig 3.1: Three transistor NAND gate schematic

The PMOS M1 and NMOS M2 on the left form a modified CMOSinverter structure. The PMOS M3 on the right acts as a pass transistor.When A=1, M3 is OFF and the modified inverter on the left (M1 and M2) functions as a normal CMOS inverter. Therefore, the output is the complement of input B.

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When A=0 and B=0, M2 is OFF, M1 and M3 are ON which leads to an undefined output state 'X',because M1 tends topull down the output node while M3 tends to pull up the output node. Similarly, when A=0 and B=1, M1 is OFF, M2 and M3 are ON leading to an undefined output state 'X',because M2 tends to pull down the output node while M3 tends to pull up the output node. For A=0 and B=0 or 1, a strong logic '1' output is required. The proposed 3T NAND gate is exempt from body bias effect, as there is no stacking of transistors. Exact output logic levels are attained for all the input combinations without any voltage degradation. An AND gate operation could be obtained with an additional CMOS inverter at the 3T NAND gate output with 5 transistors totally.

B. Three transistor-based NAND gate simulation

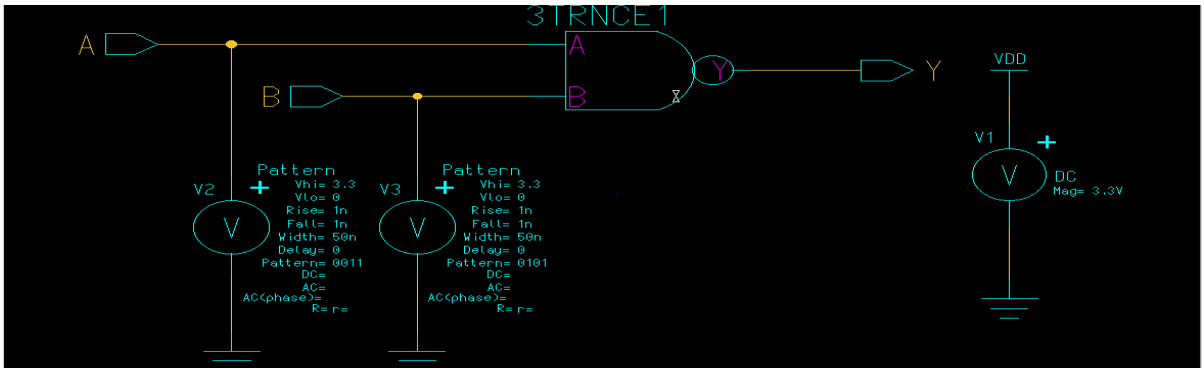

Fig 3.2: Three transistor-based NANDgate simulation

A tri-state circuit has an extra terminal where enable is connected. It behaves as a normal gate when enabled and it goes in high impedance state when disabled [9]. In literature, two MCML tri-state inverters have been proposed which are shown in the following section.

C. Three transistor-based NAND gate output waveforms

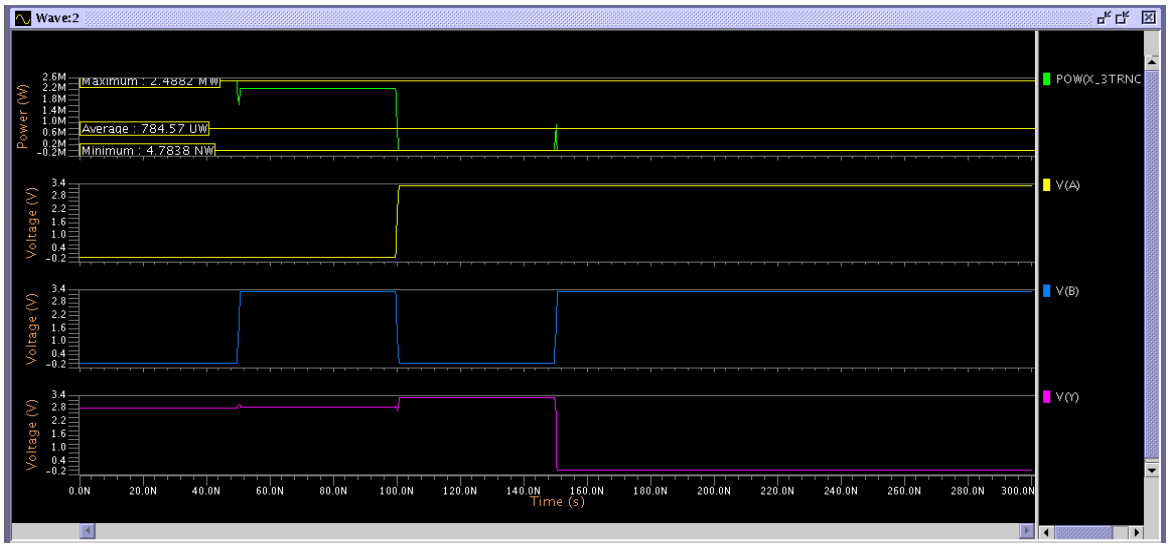

Fig 3.3: Three transistor-based NAND gate output waveforms

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D. Designing D Latch using threetransistor NAND gate

The D-latch design using tri-state inverters is given in [9]. The D-latch in [9] makes use of one inverter and two tri-state inverters shown in Fig.5 is based on CMOS. The clock signal is used to enable and disable the two inverters (I1 and I3) alternately so that one inverter is in normal mode and the other in high impedance mode or visa-versa. When clock signal is high then the input data is transferred to the output and when it is low the output state is preserved by the loop created by the two back to back inverters. The proposed D-latch design using MCML based tristate buffers require two buffers as MCML is differential logic and has both inverted and non-inverted outputs simultaneously The D-latch design for MCML based buffers. The clock signal is fed to the enable port of the two buffers operating alternately. When the clock signal is high, the buffer B1 is in normal state and the latch is transparent, thus the input is obtained at the output. The buffer B2 enters high impedance state and the loop breaks.

D .1 D Latch using three transistor NAND gate schematic

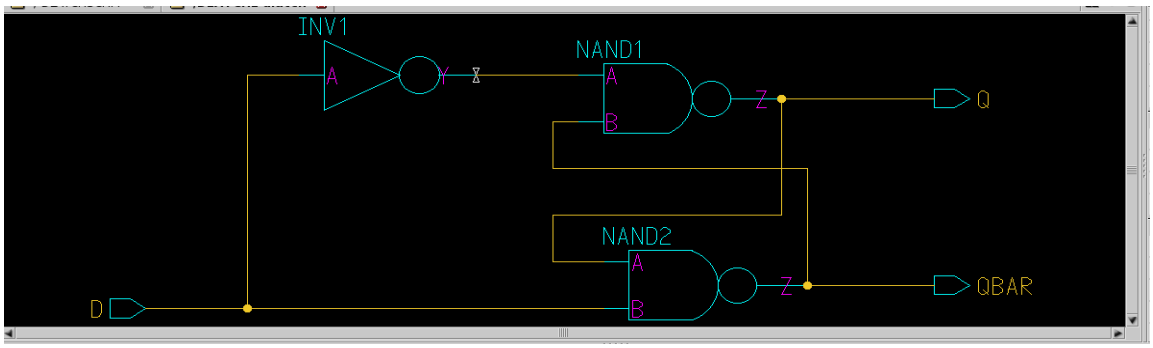

Fig 3.4.1: D Latch schematic Using three transistor NAND gate

D.2 Generating D Latch symbol

Fig 3.4.2: D Latch symbol

Semi classical two-dimensional Monte Carlo simulations provide significant evidence for ballistic devices capable of THz frequency operation in ballistic devices [8]. The modelling tool is an ensemble MC simulator of the electron dynamics self consistently coupled with a 2D Poisson solver using the finite differences approach [l0]. Comparison of experimental right drain current (left one is symmetric) as a function of the left gate voltage [10] and MC simulations is shown in Figure below.

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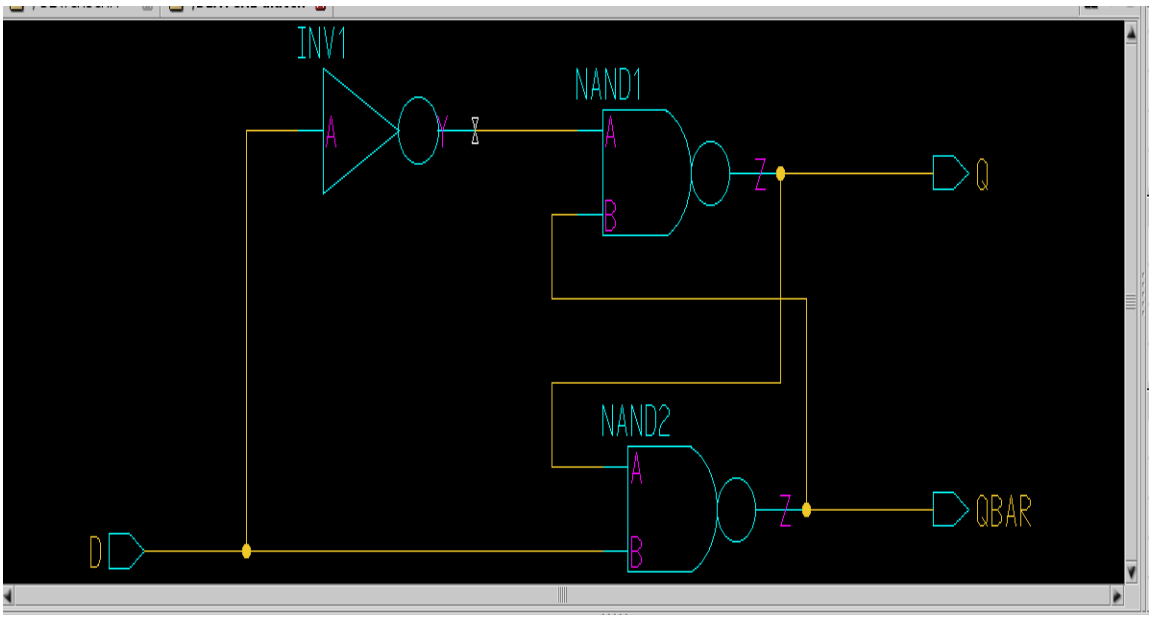
D.3 Simulation for D Latch using three transistor NAND gate



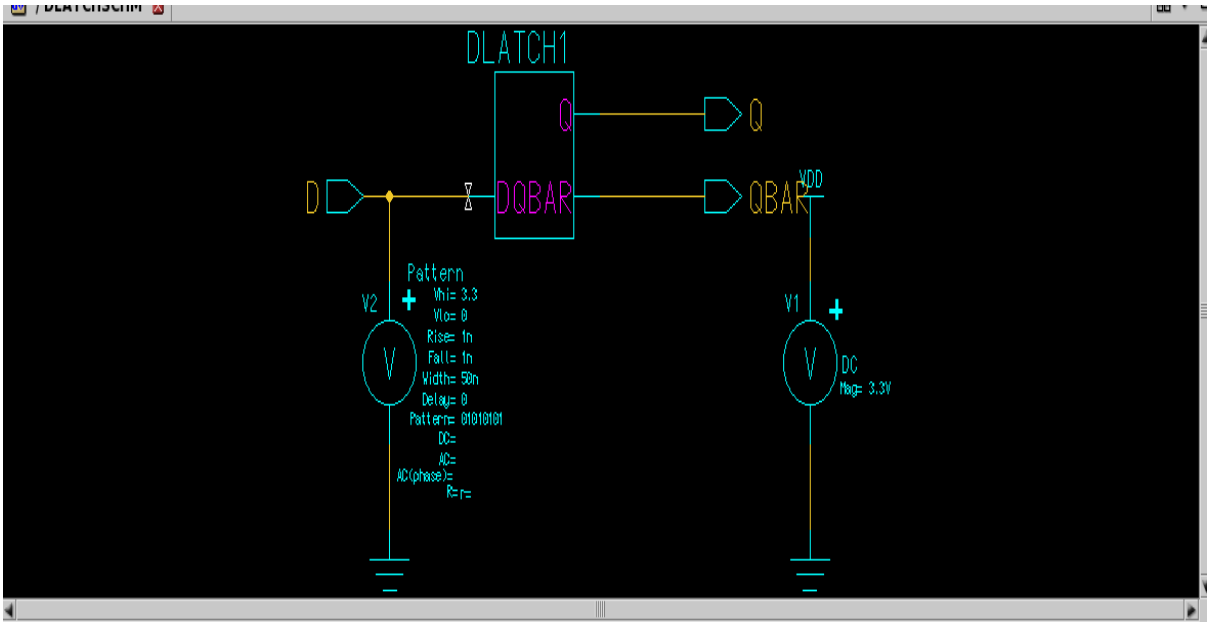


Fig 3.4.3 Simulation for D Latch using three transistor NAND gate

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D.4 D Latch using three transistor NAND gate output waveforms

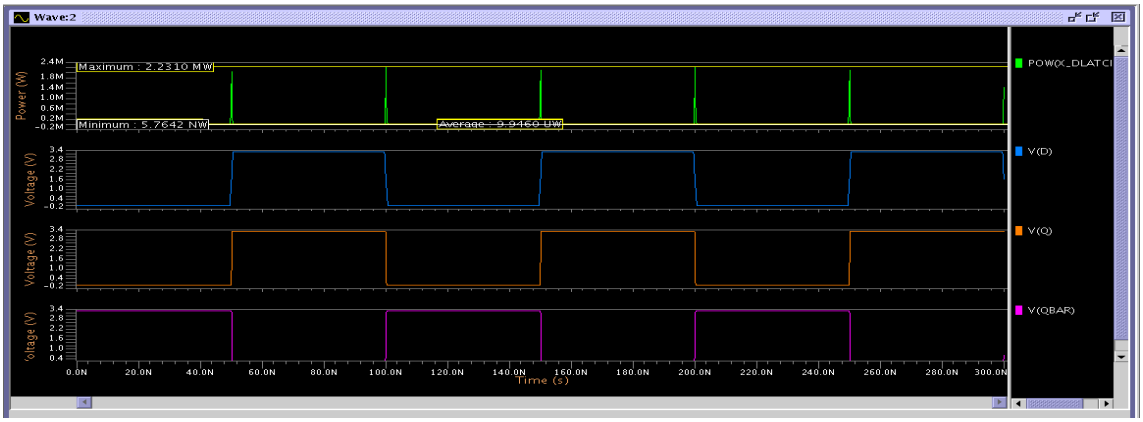

Fig 3.4.4 D Latch using three transistor NAND gate output waveforms

In order to compare the results of proposed 3T NAND gate with existing NAND gate structures, a wide range of experiments was carried out. Schematics were designed for all circuits using Custom Designer in Synopsys.

IV. CONCLUSION

A new design for D latch using 3 transistor gates is proposed and designed. Proposed design shows power consumption of 9.9469µw with supply voltage of 3.3 v .The proposed design has been compared with earlier reported with reduced output than earlier reported circuit. This is suitable for low energy application. Also, the realization of CMOS inverter given even better calculation of power delay product by rising using 130nm CMOS technology. The minimum power consumption for D latch circuit is suitable for 1.2v voltage supply. The proposed circuit improved the speed.

V. FUTURE SCOPE

Future work will improve on the results presented here, also looking into ways of removing the current-to-voltage converters and instead using the ballistic momentum to createa differential voltage across the left and right drains. We will also create additional BDT logic gates and memory elements, facilitating large-scale circuit design. With estimated operating frequencies in the hundreds of gigahertz and even terahertz, the BDT appears to be a viable option for the future ofelectronic circuit design.

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